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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/527,422	03/17/2000	Alexander I. Krymski	08305-070001	4176

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EXAMINER	
MISLEH, JUSTIN P	

ART UNIT	PAPER NUMBER
2622	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/527,422	KRYMSKI ET AL.	
	Examiner	Art Unit	
	Justin P. Misleh	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1, 2, 4, 5, 7 - 9, 15, 17, 19, 20, 40, and 41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 2, 4, 5, 7 - 9, 15, 17, 19, 20, 40, and 41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed March 29, 2007 have been fully considered but they are not persuasive.

2. Applicant argues, "Applicants respectfully submit that Sauer does not disclose, teach, or suggest clamping a capacitive storage node in a pixel signal processing circuit to a voltage less than a voltage corresponding to the pixel signal appearing on the pixel readout line, as recited in claims 1 and 15" (see Applicant's remarks, page 2, last paragraph) (emphasis added by Applicant).

3. The Examiner respectfully disagrees with Applicant's position. Sauer shows, in figure 1, an APS Pixel (110), a pixel readout line (COL_READ), and further shows a column signal processing circuit (150). Sauer additionally teaches, as shown in figure 1, wherein the signal processing circuit (150) includes a capacitive storage node (157). Moreover, Sauer additionally teach, as shown in figure 2 and as stated in column 5 (line 65) – column 6 (line 20), column 7 (lines 3 – 32), column 7 (line 60) – column 8 (line 68), clamping the capacitive storage node (157) to a voltage less than a voltage corresponds to the pixel signal appearing on the pixel readout line (The clamping is performed when the signal CL and SH are both high for ~ 1 us); subsequently coupling the pixel readout line (COL_READ) to the storage node (157; The coupling is performed when TR is at 2.5 volts, CL is low, and SH is high); and storing the pixel signal on the pixel readout line on the storage node (see column 8, lines 13 – 33). Therefore, the Examiner respectfully maintains the rejection.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 1, 2, 4, 5, 7 – 9, 15, 17, 19, 20, 40, and 41** are rejected under 35 U.S.C. 103(a) as being unpatentable over Merrill et al. (US 6,512,544 B1) in view of Sauer (US 6,320,616 B1).

6. For **Claim 1**, Merrill et al. disclose, as shown in figures 5, 7, 9, and 10 and as stated in column 6 (lines 1 – 67), column 7 (lines 52 – 67), and column 8 (lines 1 – 9 and 30 – 37), a method of processing pixel signals, the method comprising:

clamping a pixel readout line ("column line" – see figure 5) to a voltage level less than a voltage corresponding to a pixel signal (see column 6, lines 51 – 56, column 7, lines 61 – 67, and column 8, lines 1 – 6);

subsequently coupling (coupling via the rows select transistor 110) the pixel readout line ("column line") to an output of a source-follower transistor (source-follower amplifier 100) and reading out the pixel signal onto the pixel readout line ("column line"; Merrill et al. expressly state that the "COLRESET signal is asserted prior to the assertion of each ROWSEL signal"; see "integration" and "COLRESET" periods in figure 7 and also see column 8, lines 1 – 3. Furthermore, Figures 9 and 10 and column 10, lines 3 – 27, indicate a positive voltage representing the pixel signal output onto the "column line". Finally, Merrill et al. expressly state "the column line 108 may be reset to ground potential by a column-reset switch 114"; see column 6, lines 51 – 56).

While Merrill et al. disclose clamping a column bus and subsequently outputting a pixel signal to the column bus, Merrill et al. do not disclose a pixel processing circuit having a capacitive storage node, clamping the capacitive storage node to a voltage less than a voltage corresponds to the pixel signal appearing on the pixel readout line, subsequently coupling the pixel readout line to the storage node; and storing the pixel signal on the pixel readout line on the storage node.

On the other hand, Sauer also disclose a method of processing pixel signals. Specifically, Sauer shows, in figure 1, an APS Pixel (110), a pixel readout line (COL_READ), and further shows a column signal processing circuit (150). Sauer additionally teaches, as shown in figure 1, wherein the signal processing circuit (150) includes a capacitive storage node (157). Moreover, Sauer additionally teach, as shown in figure 2 and as stated in column 5 (line 65) – column 6 (line 20), column 7 (lines 3 – 32), column 7 (line 60) – column 8 (line 68), clamping the capacitive storage node (157) to a voltage less than a voltage corresponds to the pixel signal appearing on the pixel readout line (The clamping is performed when the signal CL and SH are both high for ~ 1 us); subsequently coupling the pixel readout line (COL_READ) to the storage node (157; The coupling is performed when TR is at 2.5 volts, CL is low, and SH is high); and storing the pixel signal on the pixel readout line on the storage node (see column 8, lines 13 – 33).

Therefore, at the time the invention was made, it would have been obvious to one with ordinary skill in the art to have included the pixel processing circuit including storage node that clamps the storage node and stores the pixel signal (as taught by Sauer) in the method of processing pixel signals (disclosed by Merrill et al.) for the advantage reducing the appearance of

fixed patterns noises and increasing the dynamic range is processed pixel signals (see Sauer; column 2, lines 11 – 19).

7. As for **Claim 2**, Merrill et al. disclose, as shown in figure 5 and 7 and as stated in column 6 (lines 51 – 56), wherein clamping the pixel readout line ("column line") includes discharging a capacitance (no bus capacitor or phantom bus capacitor is actually shown in figure 5; however, a bus capacitance naturally exists on the "column line" and would be discharged upon activating transistor 114) on the pixel readout line.

8. As for **Claim 4**, Merrill et al. disclose, as shown in figure 7 and as stated in column 7 (line 61) – column 8 (line 3), wherein discharging the pixel readout line ("column line") includes disabling a pixel selection switch (row select transistor 110).

As clearly shown in figure 7, the pixel (80) is completely cutoff from the column line (108) during discharging the of the column line (when "COLRESET" is asserted).

9. As for **Claim 5**, Merrill et al. disclose, as shown in figures 5 and 7 and as stated in column 7 (line 61) – column (line 3), wherein discharging the pixel readout line ("column line") includes enabling a switch to couple the pixel readout line to ground (114 – see figure 5).

10. As for **Claim 7**, Sauer additionally teaches, as shown in figure 2 and as stated in column 7 (lines 33 – 59), wherein the storage node (157) is clamped to substantially the same voltage (GROUND) and at about the same time as the pixel readout line (COL_READ).

11. As for **Claim 8**, Sauer additionally teaches, as shown in figure 1, resetting the pixel (see column 7, lines 3 – 11); subsequently reading out a reset signal through the n-MOS source-follower (see column 7, lines 3 – 11); and storing on a second capacitive storage node (C1 and

C2) in the processing circuit a signal that corresponds to the reset signal (see column 8, lines 34 – 67).

12. As for **Claim 9**, Sauer additionally teaches, as shown in figure 1, prior to storing the signal corresponding to the reset signal, clamping the second capacitive storage node to a voltage less than the voltage corresponding to the reset signal (The clamping is performed when the signal CL and SH are both high for ~ 1 us; see Column 8, lines 13 – 33); and subsequently coupling the pixel readout line to the second storage node to store the signal corresponding to the reset signal on the second storage node (see column 8, lines 34 – 67).

13. As for **Claim 40**, Merrill et al. disclose, as shown in 5, wherein the reading out of the pixel signal onto the pixel readout line ("column line") comprises reading out the pixel signal through the source-follower transistor (source-follower amplifier 100).

14. As for **Claim 41**, Merrill et al. disclose, as shown in 5, wherein the source-follower transistor (source-follower amplifier 100) comprises an n-MOS transistor.

15. For **Claim 15**, Merrill et al. disclose, as shown in figures 5, 7, 9, and 10 and as stated in column 6 (lines 1 – 67), column 7 (lines 52 – 67), and column 8 (lines 1 – 9 and 30 – 37), an imager comprising:

a pixel readout line ("column line" – see figure 5);

an active pixel sensor (see figure 5) including a source-follower transistor (source-follower amplifier 100) through which signals sensed by the sensor can be read out to the pixel readout line ("column line"), a first switch (row select transistor 110) that can be enabled to read out signals from the sensor, and a reset switch (reset transistor 88);

a controller (not explicitly shown; however, necessary for operation) configured to provide control signals to cause the pixel readout line ("column line") to be clamped to a voltage level less than a voltage corresponding to a pixel signal (see column 6, lines 51 – 56, column 7, lines 61 – 67, and column 8, lines 1 – 6), and subsequently to cause the sensor signal to be read out (coupling via the rows select transistor 110) through the source-follower transistor to the pixel readout line (Merrill et al. expressly state that the "COLRESET signal is asserted prior to the assertion of each ROWSEL signal"; see "integration" and "COLRESET" periods in figure 7 and also see column 8, lines 1 – 3. Furthermore, Figures 9 and 10 and column 10, lines 3 – 27, indicate a positive voltage representing the pixel signal output onto the "column line". Finally, Merrill et al. expressly state "the column line 108 may be reset to ground potential by a column-reset switch 114"; see column 6, lines 51 – 56).

While Merrill et al. disclose clamping a column bus and subsequently outputting a pixel signal to the column bus, Merrill et al. do not disclose a pixel processing circuit having a capacitive storage node, clamping the capacitive storage node to a voltage less than a voltage corresponds to the pixel signal appearing on the pixel readout line, subsequently coupling the pixel readout line to the storage node; and storing the pixel signal on the pixel readout line on the storage node.

On the other hand, Sauer also disclose a method of processing pixel signals. Specifically, Sauer shows, in figure 1, an APS Pixel (110), a pixel readout line (COL_READ), and further shows a column signal processing circuit (150). Sauer additionally teaches, as shown in figure 1, wherein the signal processing circuit (150) includes a capacitive storage node (157). Moreover, Sauer additionally teach, as shown in figure 2 and as stated in column 5 (line 65) – column 6

(line 20), column 7 (lines 3 – 32), column 7 (line 60) – column 8 (line 68), clamping the capacitive storage node (157) to a voltage less than a voltage corresponds to the pixel signal appearing on the pixel readout line (The clamping is performed when the signal CL and SH are both high for ~ 1 us); subsequently coupling the pixel readout line (COL_READ) to the storage node (157; The coupling is performed when TR is at 2.5 volts, CL is low, and SH is high); and storing the pixel signal on the pixel readout line on the storage node (see column 8, lines 13 – 33).

Therefore, at the time the invention was made, it would have been obvious to one with ordinary skill in the art to have included the pixel processing circuit including storage node that clamps the storage node and stores the pixel signal (as taught by Sauer) in the method of processing pixel signals (disclosed by Merrill et al.) for the advantage reducing the appearance of fixed patterns noises and increasing the dynamic range is processed pixel signals (see Sauer; column 2, lines 11 – 19).

16. As for **Claim 17**, Merrill et al. disclose, as shown in figure 5, including a third switch (114) coupled between the pixel readout line ("column line") and ground (see figure 5), wherein the controller is configured to pride a control signal (116) to cause the pixel readout line ("column line") to be clamped by enabling the third switch (see figure 7).

17. As for **Claim 19**, Sauer additionally teaches, as shown in figure 2 and as stated in column 7 (lines 33 – 59), wherein the storage node (157) is clamped to substantially the same voltage (GROUND) and at about the same time as the pixel readout line (COL_READ).

18. As for **Claim 20**, Sauer additionally teaches, as shown in figure 1, resetting the pixel (see column 7, lines 3 – 11); subsequently reading out a reset signal through the n-MOS source-

follower (see column 7, lines 3 – 11); and storing on a second capacitive storage node (C1 and C2) in the processing circuit a signal that corresponds to the reset signal (see column 8, lines 34 – 67).

Conclusion

19. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

20. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Justin P Misleh whose telephone number is 571.272.7313. The Examiner can normally be reached on Monday through Friday from 8:00 AM to 5:00 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Vivek Srivastava can be reached on 571.272.7304. The fax phone number for the organization where this application or proceeding is assigned is 571.273.8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM
April 19, 2007

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